

Design & Analysis of 16 bit RISC Processor Using low Power Pipelining

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ABSTRACT:- A 16 bit low power pipelined RISC processor is proposed by us in this paper, the RISC processor consists of the block mainly ALU, Universal shift register and Barrel Shifter. We have used modified Harvard architecture that uses separate memories for its instruction & data memory response where as in the other architecture by von Neumann, has only one shared memory for instruction and data, with one data bus and address bus with between data memory & processor memory. The remedial architectural modification has been made in incremental circuit utilized in carry select adder unit of the ALU in the RISC Processor .Operation in the core RISC Processor Fetch, Decode, execute, write back is implemented in the 2 stage pipelining with the positive edge & negative Edge .The process has been realized using XILINX ISE Design suit 13.2 & the Dynamic power is minimized in the RISC Core through the clock gating technique that is an efficient power technique and the total power estimation is done by the X Power analyzer. All the implementation is done in XILINX KINTEX XC7K1607-3fbg676 in it kit 28 nm technology are used. The simulation illustrate the total power dissipated by the processor to be 0.220 watt, and the Latency is 1.5 cycle.

Keywords:- RISC, Harvard architecture, von Neumann architecture, Latency, clock gating technique, Dynamic Power

I. INTRODUCTION

Now a day RISC Processor is increasing widely used in every field? Most microprocessor in today's market is based on either RISC or CISC architecture technologies. The RISC architecture boost the computer speed also used in control algorithms .Using of RISC Processor the time required to execute each instruction can be shortened and the number of cycles reduces. This paper depicts a RISC building design in which 2 cycle operation is gotten utilizing a pipelined outline. The pipelined architecture is used which minimizes the latency and increases the speed and in the new innovation the 2 stage pipelining which works on the positive edge and as well as in the negative edge minimizes the latency and increases the speed and also reduce the stalling in instruction. The whole architecture of RISC processor work on the 2 cycle .the fixed size of instruction allows the given instruction to be easily piped. RISC processor has a flexible architecture. The clock gating technique is used to minimize the Power. This is a most popular method to reduce the dynamic Power consumption. Power is devoured by the combinational rationale whose qualities are changing on each one clock edge so the gating rationale comes into the Picture and clock is turned off. In the present research work, the outline of 16 bit RISC processor is introduced; implemented for high efficiency and low power. The architecture supports 33 instructions. The instruction cycle consist of 2 stage pipelining and perform fetch, decode, execute, write back operation simultaneously. The control unit Generate signals from the given instructions. The architecture supports arithmetic, logical, shifting and rotation operations.

II. ARCHITETURE OF A 16 BIT RISC PROCESSOR

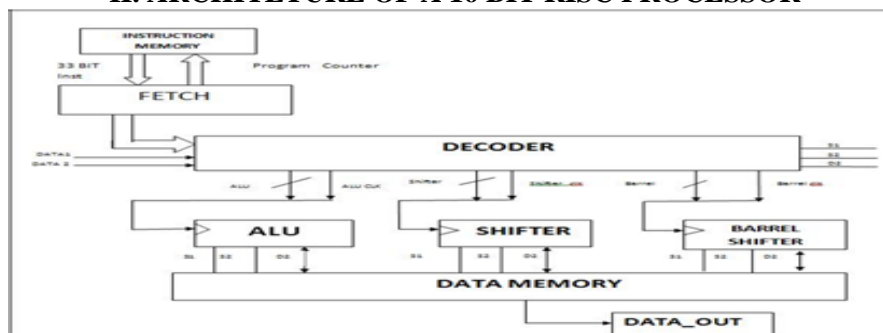


Fig. 1. Architecture of a 16 bit RISC Processor

A. Block Diagram- The construction modeling of proposed 16 bit RISC Processor comprise of ALU 1294 ISBN:978-1-4799-8890-7/15/\$31.00 ©2015 IEEE

International Conference on Computing, Communication and Automation (ICCCA2015), control unit, shifter & Barrel shifter rotator .The Design of the processor is with the Harvard architecture It can distinct program memory & data memory. In The proposed architecture 2 stage pipeline is used in the positive edge and the negative edge hence the latency is reduced and the speed is increased. The initial step in development of the processor a total of 33 instruction/operation is designed. The 2 stage pipelining carries out 4 operations Fetch, Decode, execute & read /write back. In fetch the data and instruction and are drawn from the memory. whereas in the case of decoder the data which are drawn from the memory are separated activating the three operations ALU ,shifter rotator and universal shifter register as per the requirement it may activate , through the clock gating technique saves by reducing the unnecessary switching activities. And finally in the execution, the instruction is done, the data are manipulated and the result is stored. In the 4 operations the read /write back operation are used are executed.

The ALU operation, shifter operation and shifter rotator operation are performed exactly given control signal. This operation is performed in the positive clock edge of the cycle.

- Write back- In this stage, their result is written into the register file by both single and two cycle instructions

B. Detail of logical blocks

Control unit- The control unit comprises in 2 parts of operations. In our proposed architecture the control unit work as all the coordination needed between the entire components of the processor it creates the desired control signals. It is responsible for generating the signals that decide to use.

- Fetch- Instruction memory- in the fetch33 bit of instruction are drawn from instruction memory , in the instruction memory it contains the instruction that are executed by the processor.

Program counter-The program counter contains the address of the instruction that will be fetched from the instruction memory during the next clock cycle. The pc is incremented by one during each given clock cycle. The fetch unit is work in the positive edge of the cycle.

□ Decode- In the decoder consist of 2 addressing mode as input immediate addressing mode or a register addressing mode the three operation ALU, universal shifter, shifter rotator are performed. The two decoder are exist in the control unit the first decoder perform the arithmetic and logical operation and second decoder performs rotating and shifting operations. The decoder operation is performed in negative cycle.

- Execute Unit – The execution stage is where actual computation take place. All the operations that are perform by the given control signals

C. Operations

1) ALU Operation- The ALU design has 16 operations are using ,comprises of 2 units one is for logical operation such as AND, NAND, OR, NOR, XOR, XNOR, NOT, BUFFER, Parity Generator are used and another one is arithmetic operation is used CSA Adder , subtract ,efficient multiplier and divider ,remainder, square functions are operated. IN the arithmetical logic unit the operation of Arithmetic operation such as ADD and SUBTRACT Based on the control unit operation like when

Cin=0 (Add Operation)

Cin=1 (Subtract operation)

Opcode	Source1	Source2	Destination
33 bit	9 bit	9 bit	9 bit

TABLE I. ALU Operations

SELECT LINES					DECODER															OPERATION PERFORMED		
S4	S3	S2	S1	S0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1		A0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	ADD
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SUB
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	MULTI
0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	%REM
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	AND
0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	NAND
0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	OR
0	0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	NOR
0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	XOR
0	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	XNOR
0	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	NOT
0	1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	BUFFER
0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	PARITY GENERATOR
0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DIVIDE
0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SQURE
0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	NO OPERATION

2) Universal Shift Register- The 9 operations are performed in the Universal Shift Register .The right shift operation, left shift operation and arithmetic left shift 1295

International Conference on Computing, Communication and Automation (ICCCA2015) operation is performed. Now according to the 9 select line operation performed and it is worked as follows by the table

3) Barrel shift Rotator- The input of the next multiplexer is connected to the output of first multiplexer in this way it can perform the rotation operation as the input get shifted in each multiplexer. In the barrel shifter 6 operations are performed. The left rotation and the right rotation is performed in this rotator.

TABLE II .Universal Shifter Operations

SELECT LINES									OPERATIONS PERFORMED OUTPUT
8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	1	Right Shift 1 Bit
0	0	0	0	0	0	0	1	0	Right Shift 2 Bit
0	0	0	0	0	0	1	0	0	Right Shift 3 Bit
0	0	0	0	0	1	0	0	0	Left Shift 1 Bit
0	0	0	0	1	0	0	0	0	Left Shift 2 Bit
0	0	0	1	0	0	0	0	0	Left Shift 3 Bit
0	0	1	0	0	0	0	0	0	Arithmetic Left shift1 bit
0	1	0	0	0	0	0	0	0	Arithmetic Left shift2 bit
1	0	0	0	0	0	0	0	0	Arithmetic Left shift3 bit

TABLE III. Shifter Rotator Operations

SELECT LINES						OPERATIONS PERFORMED OUTPUT
5	4	3	2	1	0	
0	0	0	0	0	1	Left Rotate 1 Bit
0	0	0	0	1	0	Left Rotate 2 Bit
0	0	0	1	0	0	Left Rotate 3 Bit
0	0	1	0	0	0	Right Rotate 1 Bit
0	1	0	0	0	0	Right Rotate 2 Bit
1	0	0	0	0	0	Right Rotate 3 Bit

III. RESULT & SIMULATION

Verilog HDL is used to describe and design The RISC Processor and is evaluated using XILINX KINTEX XC7K1607-3fbg676, 28 nm technology processor is properly validated and the simulation result show that the processor is capable of implementing on the two clock cycles. It operates at a max. frequency range of 100 MHz and the 16 bit RISC Processor using 2 stage pipeline that reduces the latency and increases the speed . A low power design technique called clock gating technique was employed to reduce the power consumption .This method drastically reduces the dynamic power to .071 w & the quiescent power is reduced to 0.149w total power consumption to 0.220w which is very less than the conventional & also final latency comes out to be 1.5 cycle.

TABLE IV. Power Dissipation

Dynamic Power	0.071
Quiescent power	0.149
Total(w)	0.220

IV. SIMULATION RESULTS



Fig.2. Simulation Waveform

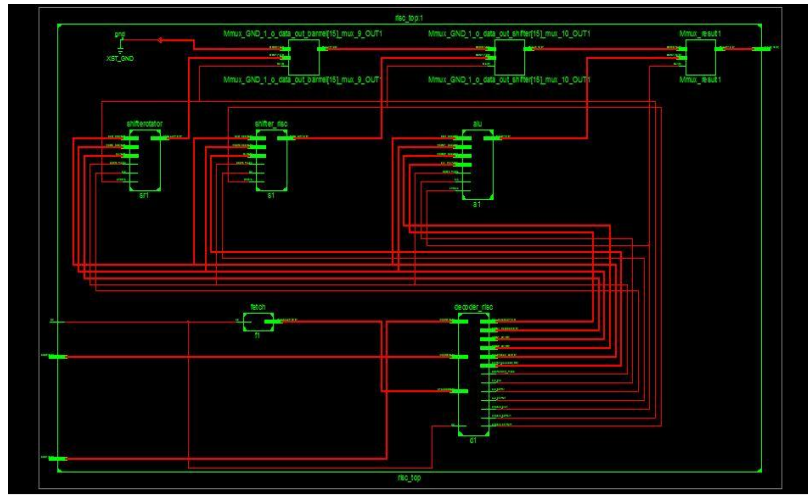


Fig.3. RTL Schematic

International Conference on Computing, Communication and Automation (ICCCA2015) flow in Verilog. One instruction takes 2 clock cycle in a 2 stage pipelining. The Carry select adder structures are employed verified through exhaustive simulation and lower power dissipation and it can increase the speed. It is expandable up to 33 instructions. Clock gating technique disabling the portion which is not required so the flip flop don't change their state and save the power. This processor can be used for the mathematical computation. It is also able to apply any control algorithm.

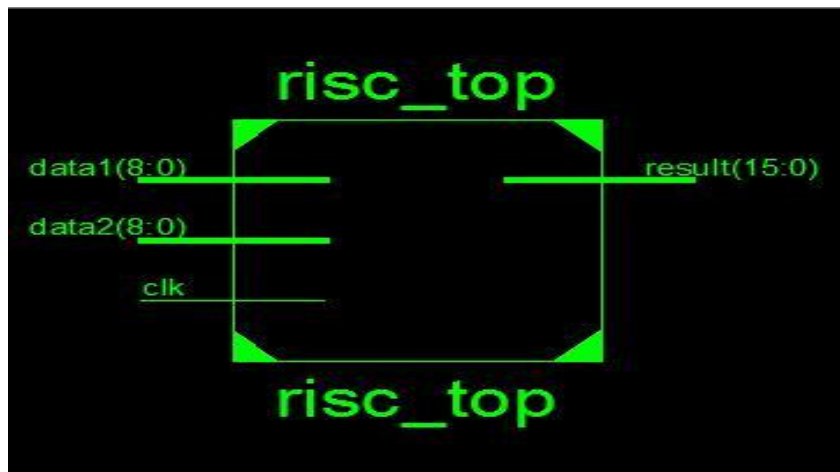


Fig.4. Technology schematic

A	B	C	D	E	F	G	H	I	J	K	L	M	N
Device		On-Chip	Power (W)	Used	Available	Utilization (%)			Supply	Summary	Total	Dynamic	Quiescent
Family	Kintex7	Clocks	0.005	1544	--	--			Source	Voltage	Current (A)	Current (A)	Current (A)
Part	xc7k160t	Logic	0.013	13382	101400	13			Vccint	1.000	0.155	0.066	0.089
Package	fbg676	Signals	0.046	37722	--	--			Vccaux	1.800	0.033	0.000	0.033
Temp Grade	Commercial	BRAMs	0.002	*	*	*			Vcco18	1.800	0.003	0.002	0.000
Process	Typical	IOs	0.005	35	400	9			Vccbram	1.000	0.001	0.000	0.001
Speed Grade	-3	Leakage	0.148										
		Total	0.219										
Environment		Thermal Properties		Effective TJA	Max Ambient	Junction Temp							
Ambient Temp (C)	25.0			(C/W)	(C)	(C)							
Use custom TJA?	No			1.9	84.6	25.4							
Custom TJA (C/W)	NA												
Airflow (LFM)	250												
Heat Sink	Medium Profile												
Custom TSA (C/W)	NA												
Board Selection	Medium (10"x10")												
# of Board Layers	12 to 15												
Custom TJB (C/W)	NA												
Board Temperature (C)	NA												
		Supply Power (W)		Total	Dynamic	Quiescent							
				0.220	0.071	0.149							

Fig.5. Power Report

V. CONCLUSION

16 bit RISC Processor having 2 stage low power pipeline is designed in this paper. Verilog Coding adopted architecture is planned in order to commend the writing code in verilog. An important role is played by Verilog coding synthesis issues in power optimally because RTL schematic depends excessively on code flow in Verilog. One instruction takes 2 clock cycle in a 2 stage pipelining .The Carry select adder structures are employed verified through exhaustive simulation and lower power dissipation and it can increases the speed. It is expandable up to 33 instructions. Clock gating technique disabling the portion which is not required so the flip flop don't change their state and save the power.

This processor can be usedfor the mathematical computation. It is also able to apply any control algorithm.

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